

# Am29501

Multi-Port Pipelined Processor (Byte-Slice™)

## DISTINCTIVE CHARACTERISTICS

- Expandable Byte-Slice™ Register-ALU
  - Sign extend input and output
  - Carry and P/G expansion with force/inhibit/normal carry modes
- Eight instruction ALU
  - Four arithmetic operations
  - Four logic operations
- Ten internal data paths
  - Highly parallel architectures
- Multiple simultaneous data manipulations
- Pipelining register file has six 8-bit registers
  - Multilevel pipelining
  - Multiple register-to-register moves
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- Three I/O ports for maximum system interconnect flexibility

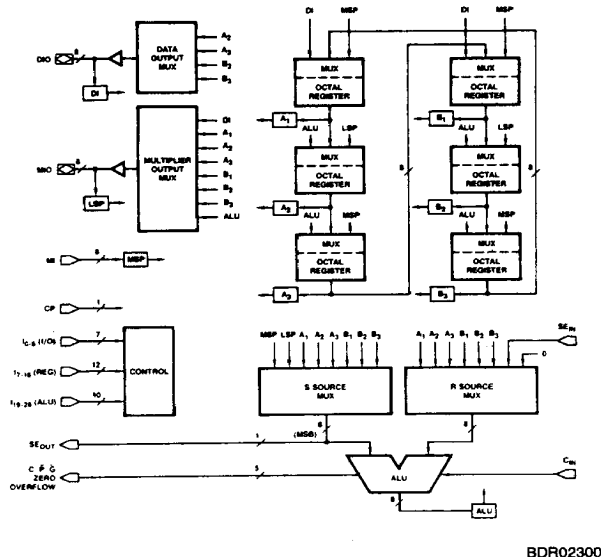
## GENERAL DESCRIPTION

The Am29501 is an expandable Byte-Slice™ register-ALU designed to bring maximum speed to array processor and digital signal processor systems. It provides a flexible processor building block for implementing highly pipelined, highly parallel architectures where speed is achieved by a combination of optimized integrated circuit technology (IMOX™ process and internal ECL circuitry) and customized system architecture. I/O port flexibility and multiple concurrent data moves make it possible to construct processors capable of very high throughput. Parallel processors are especially efficient for array/vector operations or signal processing algorithms requiring complex number arithmetic (e.g. FFT, convolution, correlation, etc.).

The Am29501's Pipeline Register File provides data storage and pipelining flexibility. Any combination of register instructions, ALU instructions, and I/O instructions can be microprogrammed to occur in the same cycle. This allows overlap of external multiplication, ALU operations, and memory I/O.

Three I/O ports support a wide variety of parallel, pipelined architectures by providing separate I/O ports for the multiplier and the memory data bus. Either of two bidirectional I/O ports, DIO and MIO, can interface to the data bus or multiplier Y-input port, and a separate MI port connects to the multiplier output port.

## BLOCK DIAGRAM



Byte-Slice is a trademark of Advanced Micro Devices, Inc.  
IMOX is a trademark of Advanced Micro Devices, Inc.

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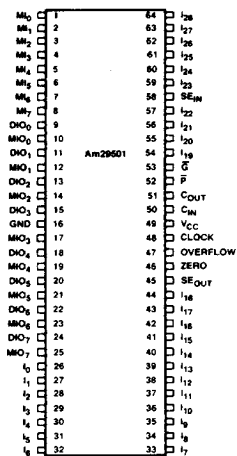
## RELATED PRODUCTS

Part No.	Description
Am2902A	Carry look-ahead generator
Am29516/17	16 x 16-bit high speed multipliers
Am25S558	8 x 8-bit multiplier

## CONNECTION DIAGRAM

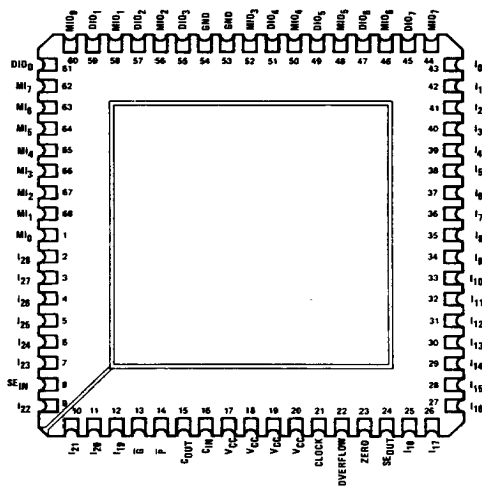
## Top View

D-64-3



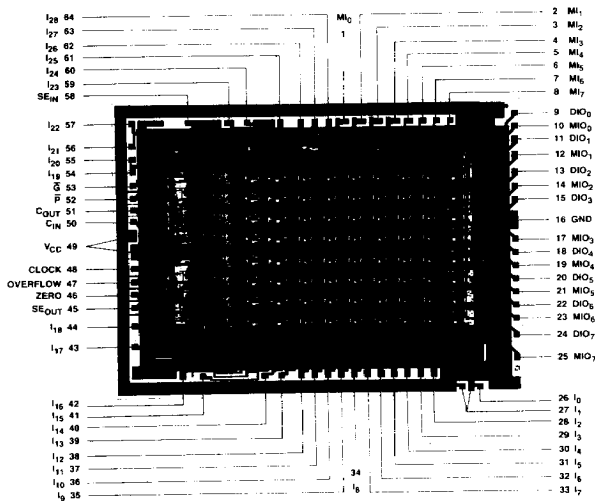
CDR04420

Leadless Chip Carrier



CDR04432

## METALLIZATION AND PAD LAYOUT



Die Size: .289" x .222"

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29501

P

C

B

Screening Option  
Blank - Standard processing  
B - Burn-in (Note 1)

Temperature (see Operating Range)  
C - Commercial (0 to +70°C)  
M - Military (-55 to +125°C)

Package

D - 64-pin Cerdip (D-64-3)  
L - 68-TERMINAL Leadless Chip Carrier

Device type

Multi-port Pipelined Processor

Note 1: 160 Hour Burn-in

Heatsink Parts,  $T_A = 125^\circ\text{C}$ Non-Heatsink Parts,  $T_A = 85^\circ\text{C}$ 

## Valid Combinations

Am29501

DC, DCB,  
DMB, LC, LMB

## Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

*Pin No.	Name	I/O	Description
50	CIN	I	Carry-in input to the internal 8-bit ALU.
51	COUT	O	Carry-out output from the internal 8-bit ALU.
48	CP	I	Clock input for the internal pipeline register file. Data selected by I <sub>7</sub> -I <sub>15</sub> , meeting the set-up and hold time requirements of the respective register, is clocked into the register on the clock LOW-to-HIGH transition.
9, 11, 13, 15, 18, 20, 22, 24	DIO <sub>0</sub> -DIO <sub>7</sub>	I/O	Bidirectional data I/O port (see Note).
53, 52	G, P	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902A for carry-lookahead.
26-44, 54-57, 59-64	I <sub>0</sub> -I <sub>28</sub>	I	Instruction inputs designed to be driven under microprogram control. All instruction inputs control multiplexers or drivers or the ALU directly. There is no instruction encoding. See Control Input Function Tables for operating modes.
1-8	MI <sub>0</sub> -MI <sub>7</sub>	I	Data Input port (Multiplier Input - see Note).
10, 12, 14, 17, 19, 21, 23, 25	MIO <sub>0</sub> -MIO <sub>7</sub>	I/O	Bidirectional data I/O port (Multiplier I/O - see Note).
47	OVR	O	Overflow This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
45	SEOUT	O	The most significant bit of the S-operand. This is used in multiple precision arithmetic operations for sign extension of two's complement numbers.
58	SEIN	I	A single-bit input which generates an 8-bit sign extension R-operand for multiple precision two's complement arithmetic operations.
46	ZERO	O	This is an open collector output which goes HIGH if the data on the ALU outputs are all LOW.

Note: This is a general purpose data port. The names are derived from the typical usage in a typical Am29500 system but are not restricted to this interconnection scheme.

\*DIP Configuration

## CONTROL INPUT FUNCTION TABLES

1. Data I/O Port (DIO) Output Select			
I <sub>3</sub>	I <sub>2</sub>	I <sub>0</sub>	Source
L	L	L	A <sub>2</sub>
L	H	L	A <sub>3</sub>
H	L	L	B <sub>2</sub>
H	H	L	B <sub>3</sub>
X	X	H	Output Disabled

2. Multiplier I/O Port (MIO) Output Select				
I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>1</sub>	Source
L	L	L	L	A <sub>1</sub>
L	L	H	L	A <sub>2</sub>
L	H	L	L	A <sub>3</sub>
L	H	H	L	B <sub>1</sub>
H	L	L	L	B <sub>2</sub>
H	L	H	L	B <sub>3</sub>
H	H	L	L	ALU
H	H	H	L	D1
X	X	X	H	Output Disabled

3. Register A <sub>1</sub> Data Source Select		
I <sub>8</sub>	I <sub>7</sub>	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	B <sub>3</sub>
H	H	A <sub>1</sub> (Hold)

4. Register A <sub>2</sub> Data Source Select		
I <sub>10</sub>	I <sub>9</sub>	Source
L	L	LSP (MIO)
L	H	ALU
H	L	A <sub>1</sub>
H	H	A <sub>2</sub> (Hold)

## CONTROL INPUT FUNCTION TABLES (Cont.)

5. Register A <sub>3</sub> Data Source Select		
I <sub>12</sub>	I <sub>11</sub>	Source
L	L	MSP (MI)
L	H	ALU
H	L	A <sub>2</sub>
H	H	A <sub>3</sub> (Hold)

6. Register B <sub>1</sub> Data Source Select		
I <sub>14</sub>	I <sub>13</sub>	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	A <sub>3</sub>
H	H	B <sub>1</sub> (Hold)

7. Register B <sub>2</sub> Data Source Select		
I <sub>16</sub>	I <sub>15</sub>	Source
L	L	LSP (MIO)
L	H	ALU
H	L	B <sub>1</sub>
H	H	B <sub>2</sub> (Hold)

8. Register B <sub>3</sub> Data Source Select		
I <sub>18</sub>	I <sub>17</sub>	Source
L	L	MSP (MI)
L	H	ALU
H	L	B <sub>2</sub>
H	H	B <sub>3</sub> (Hold)

## 9. ALU Operating Instructions

I <sub>22</sub>	I <sub>21</sub>	I <sub>20</sub>	I <sub>19</sub>	OP	COUT	P̄	Ḡ	
L	L	L	L	R + S + C <sub>IN</sub> R - S - C <sub>IN</sub> R + C <sub>IN</sub> -R + S - C <sub>IN</sub>	Carry	P̄	Ḡ	Normal Operating Mode**
L	L	L	H	R + S + C <sub>IN</sub> R - S - C <sub>IN</sub> R + C <sub>IN</sub> -R + S - C <sub>IN</sub>	L	H	H	Inhibit Carry Mode
L	L	H	L	R + S + C <sub>IN</sub> R - S - C <sub>IN</sub> R + C <sub>IN</sub> -R + S - C <sub>IN</sub>	H	P̄	L	Force Carry Mode
L	L	H	H	R XOR S R AND S R̄ R OR S	(L)*	(H)*	(H)*	Logic Operations

\*COUT, P̄ and Ḡ are not applicable to logic operation, Am29501 functions as shown.

\*\*Carry is used for 16-bit expansion. P̄ and Ḡ are used with an Am2902A for expansion to more than 16 bits.

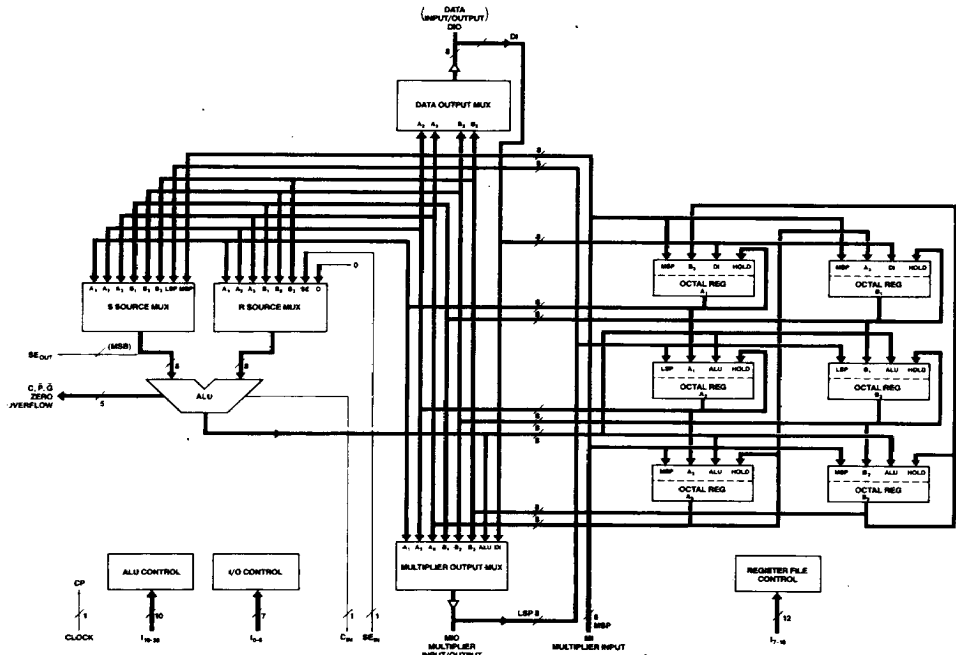
10. ALU R Operand Selection			
I <sub>25</sub>	I <sub>24</sub>	I <sub>23</sub>	Source
L	L	L	A <sub>1</sub>
L	L	H	A <sub>2</sub>
L	H	L	A <sub>3</sub>
L	H	H	B <sub>1</sub>
H	L	L	B <sub>2</sub>
H	L	H	B <sub>3</sub>
H	H	L	Sign Extend Input Bussed to All Bits
H	H	H	Arithmetic Zero (All Inputs LOW)

11. ALU S Operand Selection			
I <sub>28</sub>	I <sub>27</sub>	I <sub>26</sub>	Source
L	L	L	A <sub>1</sub>
L	L	H	A <sub>2</sub>
L	H	L	A <sub>3</sub>
L	H	H	B <sub>1</sub>
H	L	L	B <sub>2</sub>
H	L	H	B <sub>3</sub>
H	H	L	MSP (MI)
H	H	H	LSP (MIO)

## DETAILED DESCRIPTION

Figure 1 contains a block diagram of the Am29501. It shows four major sections – an eight-bit cascadable ALU, a register file consisting of six eight-bit registers, three I/O ports, and a microcode control section.

DETAILED Am29501 BLOCK DIAGRAM



DFR00710

Figure 1.

### ALU

The ALU performs arithmetic on an eight-bit Byte-Slice™ with full internal carry lookahead and carry input and output for cascading. The carry can ripple between byte-slices by connecting the C<sub>OUT</sub> of one slice to C<sub>IN</sub> of the next byte-slice. Carry generate (G) and propagate (P) outputs are also provided for faster operation when the ALU is used in conjunction with a carry lookahead generator such as the Am2902A.

There are three arithmetic modes – cascade, carry inhibit and forced carry. The cascade mode produces an output carry based on the results of the operation and is the normal mode. The carry inhibit mode produces no carry output and is used to decouple cascaded ALUs. A 16-bit ALU consisting of two Am29501s can operate as two 8-bit ALUs simultaneously by programming the carry inhibit mode. This mode could also be used with a second 16-bit ALU for double precision where the more significant slice is programmed in the carry inhibit mode for single precision and in the cascade mode for double precision. The less significant slices would be programmed in normal mode for either case. The forced carry mode is the

converse and always produces a carry. All three modes treat the input carry in the same way. The Am29501 uses the input carry as a true borrow during subtraction as opposed to most two's complement ALUs which use borrow. The usual requirement is that input borrow be programmed HIGH (inactive) when doing a subtraction. Since the Am29501 has a true borrow, the input carry is programmed to be LOW for both addition and subtraction. This is consistent with the carry inhibit mode discussed previously.

In addition to arithmetic operations the ALU also does bitwise logic operations – OR, AND, exclusive OR, and invert. Carries are not applicable for these operations and are inactive. Codes to program the ALU function are contained in Control Input Function Table 9.

Each operand of the ALU has eight possible sources. Operand R can be any register in the register file or one of the I/O ports MI or MIO as shown in Table 10. Operand S can be any register, zero or a sign extension input (SE<sub>IN</sub>) from another ALU (Table 11). The ALU result can be steered to registers A2, A3, B2, and B3 of the register file or the MIO I/O port.

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## REGISTER FILE

The register file provides for fully independent use of the registers. Each register has a four-input mux which can be programmed so that the register holds its previous contents or is loaded from the ALU and I/O port or the "preceding" register. If all registers are programmed for the preceding register, a ring is formed and data circulates through all the registers. This facilitates constructing a pipelined data flow. Various combinations of I/O ports and the ALU make up the remaining inputs to each register. The sources for each register are shown in the Control Input Function Tables 3-8.

## I/O PORTS

The Am29501 has two bidirectional ports (DIO and MIO) and one input port (MI). As an input the DIO port can be loaded into registers A1 and B1 and directed to the MIO output port. Output from the DIO comes from registers A2, A3, B2 or B3 using the codes from Control Input Function Table 1. This separation of input and output registers connected to the DIO port is in keeping with the pipelined organization of the part when the DIO port is used for data flow in and out of the processor.

Input through the MIO port can be directed to registers A2 and B2 in the register file and to the ALU. Output can come from any of the six registers, the DIO input port or from the ALU.

This structure allows the user to direct operands to an auxiliary processor (such as a multiplier or barrel shifter) from any point in the pipeline. The MIO port could be connected to a processor with bidirectional data bus. The auxiliary processor would receive data and return its results to registers A2 and B2 through the MIO port.

The MI port provides another entry point for inserting data in the processing pipeline. An auxiliary processor with flow-through architecture could receive data from the MIO port and return data through the MI port which can be directed to registers A1, A3, B1 and B3 and to the ALU.

A potential use of the ports is connecting the bidirectional bus of an Am29116 microprocessor to the MIO port. An Am29516 would have its inputs connected to the same MIO port and its output to the MI port. This architecture could calculate magnitudes by computing the sum of the squares with the Am29516 and Am29501 and the square root with the Am29116.

## CONTROL

The Am29501 is controlled by 29 microcode bits which select operations with no encoding. This provides the maximum flexibility for the independent control of parallel operations. Sources may be directed to multiple destinations simultaneously wherever data paths are provided.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature ..... -65 to +150°C  
 Temperature Under Bias- $T_C$  ..... -55 to +125°C  
 Supply Voltage to Ground Potential  
   Continuous ..... -0.5 to +7.0V  
 DC Voltage Applied to Outputs For  
   High Output State ..... -0.5V to + $V_{CC}$  max  
 DC Input Voltage ..... -0.5 to +5.5V  
 DC Output Current, Into Outputs ..... 30mA  
 DC Input Current ..... -30 to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

**OPERATING RANGES****Commercial (C) Devices**

## Temperature

DIPs .....  $T_A = 0^\circ\text{C}$  to +70°CChip Carriers .....  $T_C = 0^\circ\text{C}$  to 85°C

Supply Voltage ..... +4.75V to +5.25V

**Military (M) Devices**

Temperature ..... -55°C to +125°C

Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

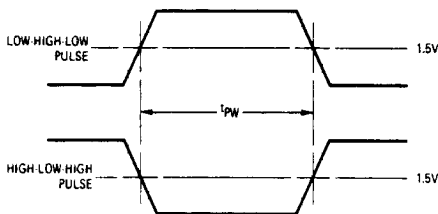
**DC CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or $V_{IL}$		$I_{OH} = -2.6\text{mA}$ (COM'L)	2.4		Volts
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{MIN}$ $V_{IN} = V_{IH}$ or $V_{IL}$	COM'L	$I_{OL} = 24\text{mA}$ DIO, MIO		0.5	Volts
				$I_{OL} = 8\text{mA}$ Others		0.5	
			MIL	$I_{OL} = 16\text{mA}$ DIO, MIO			
				$I_{OL} = 8\text{mA}$ Others		0.5	
$V_{IH}$	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
$V_{IL}$	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					Volts
$V_i$	Input Clamp Voltage	$V_{CC} = \text{MIN}$ , $I_{IN} = -18\text{mA}$				-1.5	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 0.5\text{V}$				-0.4	mA
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 2.7\text{V}$				20	$\mu\text{A}$
$I_i$	Input HIGH Current	$V_{CC} = \text{MAX}$ , $V_{IN} = 5.5\text{V}$				0.1	mA
$I_{OZH}$	Off State (High Impedance) Output Current	$V_{CC} = \text{MAX}$	$V_O = 0.5\text{V}$			-55	$\mu\text{A}$
$I_{OLZ}$			$V_O = 2.4\text{V}$			100	
$I_{SC}$	Output Short Circuit Current (Note 3)	$V_{CC} = \text{MAX}$		-30		-100	mA
$I_{CC}$	Power Supply Current	COM'L and MIL		$T_A = 25^\circ\text{C}$	300		mA
		COM'L Only		$T_A = 0$ to +70°C (Note 4)		400	
		$V_{CC} = \text{MAX}$		$T_A = +70^\circ\text{C}$ (Note 4)		375	
		MIL Only		$T_C = -55$ to +125°C			
		$V_{CC} = \text{MAX}$		$T_C = +125^\circ\text{C}$			

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.  
 2. Typical limits are at  $V_{CC} = 5.0\text{V}$ , 25°C ambient and maximum loading.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4. Chip Carriers:  $T_C = 85^\circ\text{C}$ .

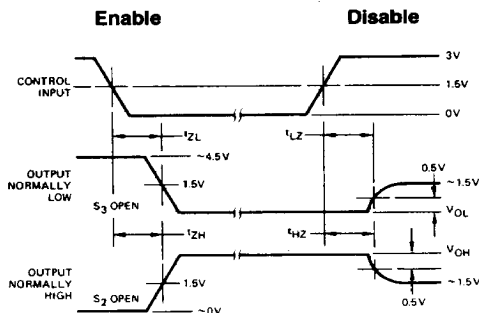


## PULSE WIDTH



WFR02790

## ENABLE AND DISABLE TIMES



WFR02660

- Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.  
2. S<sub>1</sub>, S<sub>2</sub> and S<sub>3</sub> of Load Circuit are closed except where shown.

NOTE: 1. Pulse generator for all pulses: Rate  $\leq 1.0\text{MHz}$ ; Z<sub>O</sub> = 50 $\Omega$ ; t<sub>r</sub>  $\leq 2.5\text{ns}$ ; t<sub>f</sub>  $\leq 2.5\text{ns}$ .

## SWITCHING CHARACTERISTICS AT ROOM TEMPERATURE

Typical Set-up/Hold Times and Propagation Delays  
V<sub>CC</sub> = 5.0V, T<sub>A</sub> = + 25°C, C<sub>L</sub> = 50pF

To Output													Units
From Input	Set-up, $t_s$ /Hold, $t_h$		Propagation Delay Times, $t_{pd}$										
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	COUT	P	G	Z	Overflow	SEOUT		
CLK			17	27	17	23	23	23	27	34	18	ns	
DIO			12									ns	
MIO						22	22	22	25	22	17	ns	
MI				24		22	22	22	25	22	17	ns	
CIN				16		10			17	13		ns	
SEIN				23		19	19	16	22	19		ns	
I2-3(DIO)												ns	
I4-6(MIO)												ns	
I7-18(REG)												ns	
I19-22(ALU OP)						19	19	19	22	19		ns	
I23-28(ALU SEL)				31		20	20	20	25	22	14	ns	

## Am29501 Three-State Timing

Parameters	Description	Test Conditions	Typ	Max	Commercial	Military	Units
			V <sub>CC</sub> = 5V T <sub>A</sub> = 25°C	V <sub>CC</sub> = 5V T <sub>A</sub> = 25°C	Max	Max	
t <sub>LZ</sub>	I <sub>0</sub> → DIO <sub>0-7</sub>	C <sub>L</sub> = 5pF R <sub>L</sub> = 667 $\Omega$	10		15		ns
	I <sub>1</sub> → MIO <sub>0-7</sub>						
t <sub>HZ</sub>	I <sub>0</sub> → DIO <sub>0-7</sub>	C <sub>L</sub> = 5pF R <sub>L</sub> = 667 $\Omega$	10		15		ns
	I <sub>1</sub> → MIO <sub>0-7</sub>						
t <sub>ZL</sub>	I <sub>0</sub> → DIO <sub>0-7</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 667 $\Omega$	12		20		ns
	I <sub>1</sub> → MIO <sub>0-7</sub>						
t <sub>ZH</sub>	I <sub>0</sub> → DIO <sub>0-7</sub>	C <sub>L</sub> = 50pF R <sub>L</sub> = 667 $\Omega$	12		20		ns
	I <sub>1</sub> → MIO <sub>0-4</sub>						

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**SWITCHING CHARACTERISTICS, COMMERCIAL****Minimum Set-up/Hold Times and Maximum Propagation Delays**

From Input	To Output											Units
	Set-up, $t_s$ /Hold, $t_h$		Propagation Delay Times, $t_{PD}$									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	COUT	P	Q	Z	Overflow	SEOUT	
CLK			23	35	24	31	31	31	39	34	26	ns
DIO	10/5		17									ns
MIO	10/5	20/0				29	29	29	34	29	24	ns
MI	10/5	20/0		32		30	29	29	34	29	24	ns
CIN		10/5		25		15			26	19		ns
SEIN		20/0		29		27	27	22	32	27		ns
I2-3(DIO)					21							ns
I4-6(MIO)			22									ns
I7-18(REG)	10/5											ns
I19-22(ALU OP)		20/0	32			27	27	27	32	29		ns
I23-28(ALU SEL)		20/0				29	29	29	35	32	22	ns

**SWITCHING CHARACTERISTICS, MILITARY****Minimum Set-up/Hold Times and Maximum Propagation Delays**

From Input	To Output											Units
	Set-up, $t_s$ /Hold, $t_h$		Propagation Delay Times, $t_{pD}$									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	COUT	P	G	Z	Overflow	SEOUT	
CLK												ns
DIO												ns
MIO												ns
MI												ns
CIN												ns
SEIN												ns
I2-3(DIO)												ns
I4-6(MIO)												ns
I7-18(REG)												ns
I19-22(ALU OP)												ns
I23-28(ALU SEL)												ns

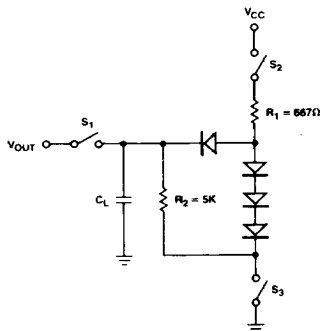
Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in section 13 of this data book.

**Am29501 Minimum Clock Pulse Widths**

Parameter	Description		TYPICAL	COMMERCIAL	MILITARY	Units
tpw	Clock Pulse Width	High		15		ns
		Low		15		ns

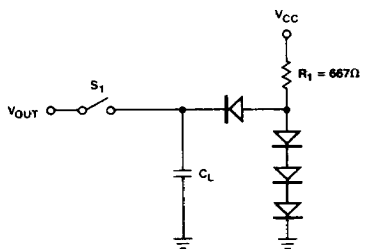
## SWITCHING TEST CIRCUIT

## A. THREE-STATE OUTPUTS



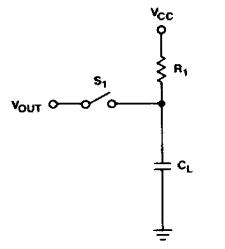
TCR01330

## B. NORMAL OUTPUTS



TCR01340

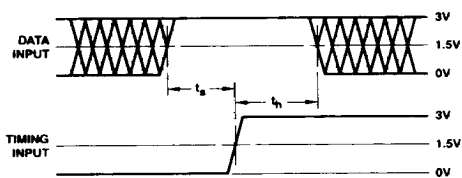
## C. OPEN-COLLECTOR OUTPUTS



TC001420

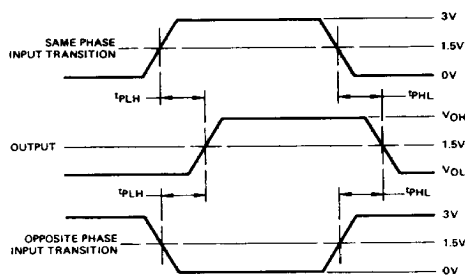
- Notes: 1.  $C_L = 50\text{pF}$  includes scope probe, wiring and stray capacitances without device in test fixture.  
 2.  $S_1, S_2, S_3$  are closed during function tests and all AC tests except output enable tests.  
 3.  $S_1$  and  $S_3$  are closed while  $S_2$  is open for  $t_{pZH}$  test.  
 $S_1$  and  $S_2$  are closed while  $S_3$  is open for  $t_{pZL}$  test.  
 4.  $C_L = 5.0\text{pF}$  for output disable tests.

## SET-UP, HOLD, AND RELEASE TIMES



WFR02970

## PROPAGATION DELAY



WFR02980

- Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.  
 2. Cross hatched area is don't care condition.



$C_i \cong 5.0\text{pF}$ , all inputs



$C_O \cong 5.0\text{pF}$ , all outputs  
Note: Actual current flow direction shown.